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CARMA First-Light Correlator Spectral-line Configurations

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ABSTRACT

The spectral-line capabilities of an interim CARMA correlator based on an expansion of the current COBRA digital hardware is discussed. It is found that the COBRA correlator FPGAs can support the previously proposed channel resolutions for the widest bandwidths (16 channels @ 500 MHz and 32 channels @ 250 MHz), whereas for narrower bandwidths the maximum resolution is a factor of two below the original estimates (64 channels @ 8 and 2 MHz). It may be possible to increase resolution by using higher density FPGAs in new correlator cards; however, the concomitant increase in power dissipation is a serious concern, and careful study would be needed to determine its feasibility. Alternatively, additional bands could be added (proportionately increasing hardware costs).

1. The Interim CARMA Correlator

Beasley, Woody, and Hawkins (2002) have outlined a plan for the CARMA first-light correlator based on the existing COBRA design. In this plan additional digitizer and correlator cards, identical in design to the latest revision COBRA hardware, would be used to implement an interim correlator for CARMA with 4 GHz total bandwidth (8 bands of 500 MHz each). The suitability of COBRA digital hardware (at the FPGA level) for this wideband configuration has already been verified (Rauch 2002); additional testing using live hardware is pending.

Several issues remain regarding the design specifications of the first-light correlator. Here we focus attention on the spectral-line capabilities of the COBRA correlator card FPGAs, and determine the number of channels they can support. Related unresolved matters, such as the correlator DSP utilization implied by these results, may force a small reduction (<10%) in the number of channels available in some spectral modes. Implementation of any particular mode is also contingent upon its availability in the first-light digitizers and downconverters.

2. Simulation of CARMA Spectral-line Capabilities

In terms of the correlator FPGAs, the basic task is to determine the total number of lags (channels) that can be processed by a single FPGA in real time. Note that for CARMA, all lags for a given baseline are processed by one FPGA (COBRA allocates two FPGAs per baseline); hence the number of channels per baseline is half that of COBRA for the same bandwidth. The CARMA wideband configuration (500 MHz bandwidth per window) analyzed previously supports 16 channels per sideband, consistent with the original projections. In this mode, the correlation logic inside the FPGAs runs at 125 MHz (the maximum rate) and processes data that has been demultiplexed at the digitizers by a factor of 8 (DEMUX = 8). Because of the additional logic required to process demultiplexed samples in parallel, maximizing NLAGS—the number of lags computed by an FPGA—requires using the least possible amount of demultiplexing. The accessible region of the "DEMUX-NLAGS plane" satisfies two basic constraints: first, the correlation logic is able to operate at the required clock frequency (i.e., to correlate the data in real time), and second, it can be placed and routed successfully within the device. The first constraint dominates for wide bandwidths (DEMUX > 1) and the second for narrow ones (DEMUX = 1).

To ascertain the maximum value of NLAGS for each proposed CARMA spectral-line bandwidth, the CARMA wideband VHDL codebase was generalized and a series of simulations were performed to determine the maximum value of NLAGS for which the constraints mentioned above could be met; in each case the DEMUX factor was set to the lowest value possible given an operating frequency of 125 MHz—the highest supported by the COBRA correlator cards. It turned out that one synthesis option, the extent to which the component hierarchy was preserved during logic synthesis (the process by which high-level VHDL code is translated into low-level logic gates), had a significant impact on the maximum operating frequency of the final circuit. In particular, for large DEMUX factors (wide bandwidth) a highly flattened design produced the best results, while for DEMUX = 1 (narrow bandwidth) the reverse was true. This added an additional search dimension to the simulations, one which was crudely (though adequately) sampled as part of the analysis to keep the required CPU times reasonable. After maximizing NLAGS, full timing simulations for each combination of bandwidth and FPGA routing solution (see Rauch 2002) were performed to verify proper operation of the correlator card as a whole.

3. Discussion

The simulation results are summarized in Tables 1 and 2. Table 1 displays the number of channels (per sideband) that can be implemented using COBRA hardware for each spectral bandwidth, along with the corresponding channel spacings and total velocity widths for observations taken at either 3 mm or 1 mm. Table 2 details the VHDL parameters used in the corresponding timing simulations, including overall device utilization.

The simulations show that the originally proposed channel resolutions can be met for bandwidths of 512 and 256 MHz; for narrower bandwidths, the number of available channels increases more slowly. The critical bandwidth in terms of satisfying the constraints was 64 MHz, the widest one permitting DEMUX = 1; in this case it was necessary to significantly reduce the number of lags (relative to what could be placed and routed) in order to meet timing. If narrowband resolutions are deemed insufficient, there are two possible ways to increase resolution without radically changing the design. One is simply to increase the number of bands (windows) beyond 8, increasing the available number of channels, the total frequency coverage, and the hardware costs proportionately. The other is to load new correlator cards with FPGAs twice as dense (i.e., containing double the number of logic elements) as those used for COBRA; however, this would also approximately double the power dissipation of the cards, and it is not clear whether this is feasible within the current design. Additional analysis would be required to determine the viability of this latter option. But if practical, it would be the more cost-effective of the two options, since additional crates, downconverters, digitizers, etc., are not required to implement it; on the other hand, total frequency coverage does not increase. Should digital FIR filtering inside the digitizers (currently under study) prove to be feasible, it may even be possible to implement a 1 MHz bandwidth mode to increase the maximum attainable velocity resolution, albeit with an equal reduction in total frequency coverage.

REFERENCES

Beasley, A.J., Woody, D.P., and Hawkins, D.W., 2002, CARMA Memo 3.
Rauch, K.P., 2002, CARMA Memo 7.

Table 1. Single-window spectral resolutions for a COBRA-based interim correlator [a]

Bandwidth (MHz)	Channels (per sideband)	δV[3 mm] (km/s)	$V_{\rm tot}$[3 mm] (km/s)	δV[1 mm] (km/s)	$V_{\rm tot}$[1 mm] (km/s)
512	16	96	1536	32	512
256	32	24	768	8	256
128	40	9.6	384	3.2	128
64	48	4	192	1.3	64
32	56	1.7	96	0.57	32
8	64	0.38	24	0.13	8
2	64	0.09	6	0.03	2

[a] A total of eight individually configurable 500 MHz bands (“windows”), each with two (non-contiguous) sidebands, are available in the proposed plan, allowing many possibilities for channel spacing and total frequency coverage.

Table 2. VHDL simulation parameters for the CARMA spectral-line analysis

Bandwidth (MHz)	`NUM_LAGS`	`CORL_DEMUX` (@MHz)	`PRESCALER WIDTH`	`COUNT WIDTH`	utilization[a] (%)	min(fmax)[b] (MHz)
512	20	8(@125)	3	17	95	135
256	32	4(@125)	3	17	96	137
128	44	2(@125)	3	17	97	124
64	48	1(@125)	3	17	83	135
32	60[c]	1(@62.5)	2	17	97	99
8	68[c]	1(@15.6) [d]	0	17	91	68
2	72[c]	1(@3.9) [d]	0	15	90	77

[a] Maximum fraction of FPGA logic cells used.

[b] Worst-case correlation logic operating frequency.

[c] Place and route stage nearly failed.

[d] Requires divided clock (or equivalent).