CPLD signals and interfaces

A. Harris, September 28, 2007, CPLD code version 3.0

1 Internal registers

Table 1: CPU writes to control register 0 (bits_out0) at address = base + 0. Default setup value = 0x0A80.

Bit	Name	Description	Default
0	master	set high if master, low if slave	0
1	sync_enable	if slave, pulse high for $\geq$ 30 ms to synchronize system clocks	0
2	read_low_bits	set low for normal operation	0
3	noise_diode0	set high to synchronously fire noise diode 0	0
4	phase switch mode	set high for quadrature modulation	0
5	periph_clk	serial clock for peripherals (e.g. attenuators)	X
6	periph_dout	serial data for peripherals	X
7	periph_sel0	set low to select attenuator0	1
8	periph_sel1	set low to select attenuator1	1
9	periph_sel2	set low to select monitor point ADC	1
10	periph_sel3	set high to jam noise diode on	0
11	blank	set low when correlator data acquision is active	1
12	nodB	nod signal for beam B (CSO)	0
13	nodA	nod signal for beam A (CSO)	0
14	chop	chop switching signal (CSO)	0
15	int_reset	CPLD internal reset	0

Table 2: CPU writes to control register 1 (bits_out1) at address = base + 1. Default setup value = 0xff.

Bit	Name	Description	Default
0	setup_dclk	micro-generated clock for ADC setup	X
1	reset_adc_system	reset line to ADC system	1
2	reset_adc_setup	reset internal ADC setup	1
3	r_sup	run or setup mode for ADC system	1
4	setup	setup data to ADC system	X
5	osc_enable	enables 2 MHz oscillator	1
6	external phase switch	enables differential phase switch driver	1
7	internal phase switch	enables internal phase switch driver	1

Table 3: CPU reads from bits_in at address = base + 0

Bit	Name	Description
0	first_in_frame	high for first interrupt of correlator ADC readout
1	frame	frame signal
2	periph_din	serial data from peripherals
3	serial_in0	serial data from correlator bank 0
4	serial_in1	serial data from correlator bank 1
5	ext_blank	read blank signal from master when slave
6	ext_nod_b	read nodB signal from master when slave
7	ext_nod_a	read nodA signal from master when slave
8	ext_chop	read chop signal from master when slave
9	jumper_0	jumper 0 on PCB
10	jumper_1	jumper 1 on PCB
11	jumper_2	jumper 2 on PCB
10	ver_0	CPLD code version number bit (LSB)
13	ver_1	CPLD code version number bit
14	ver_2	CPLD code version number bit
15	ver_3	CPLD code version number bit (MSB)

Table 4: CPU reads previous parallel data from serial_0 at address = base + 1

Bit	Name	Description
0-15	ADC word	ADC readout word from correlator bank 0

Table 5: CPU reads previous parallel data from serial_1 at address = base + 2

Bit	Name	Description
0-15	ADC word	ADC readout word from correlator bank 1

Table 6: CPU reads current parallel data from serial_0 at address = base + 3

Bit	Name	Description
0-15	ADC word	ADC readout word from correlator bank 0

Table 7: CPU reads current parallel data from serial_1 at address = base + 4

Bit	Name	Description
0-15	ADC word	ADC readout word from correlator bank 1

Table 8: CPU reads control register 0 at address = base + 8

Table 9: CPU reads control register 1 at address = base + 9

Table 10: Monitor point ADC

Channel	Description	Conversion
0	Aux. interface card temperature	°C = (counts − 500)/10
1	Correlator card temperature	°C = (counts − 500)/10
2	Amp module 1 temperature	°C = (counts − 500)/10
3	Amp module 2 temperature	°C = (counts − 500)/10
4	+3.3 V	V = counts/1000
5	+5 V	V = counts/589
6	−5 V	V = counts/204
7	15 V	V = counts/204

Table 11: CPLD writes to logic analyzer (pin assignments match Agilent 20-pin header)

Bit	Name	Description
0	D0	
1	D1	
2	D2	
3	D3	
4	D4	
5	D5	
6	D6	
7	D7	
8	D8	